Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.014”**

**.014”**

**EMITTER**

**.0025 X .008”**

**B**

**.0025”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: B = .0025” X .0025”**

**E = .0025” X .008”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .014” X .014” DATE: 9/23/21**

**MFG: SILICON SUPPLIES THICKNESS .006” P/N: BRF391**

**DG 10.1.2**

#### Rev B, 7/1